# CMOS Hex Buffer/Converters

## 1. Description

The CD4049UB and CD4050B are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage ($V_{CC}$). The input-signal high level ($V_{IH}$) can exceed the $V_{CC}$ supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads.

## 2. Features

- CD4049UB Inverting
- CD4050B Non-Inverting
- High Sink Current for Driving 2 TTL Loads
- High-To-Low Level Logic Conversion
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and 25°C
- 5V, 10V and 15V Parametric Ratings

## 3. Applications

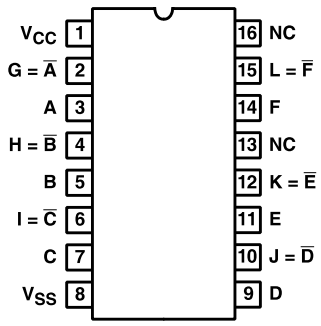
- CMOS to DTL or TTL Hex Converters
- CMOS Current Sink or Source Drivers
- CMOS High-to-Low Logic Level Converters

## 4. Ordering Information

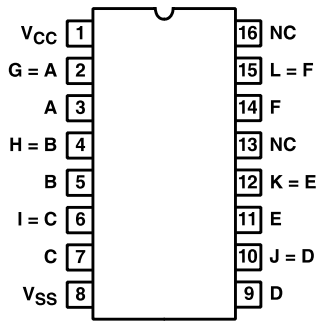
| Type Number | Description | Package Type | Marking | Packing | SPQ |
|---|---|---|---|---|---|
| CD4049UBN | | DIP-16 | CD4049UB | Tube | |
| CD4049UBM | | SOP-16 | CD4049UB | Reel | |
| CD4050BN | | DIP-16 | CD4050B | Tube | |
| CD4050BM | | SOP-16 | CD4050B | Reel | |

## 5. Pinouts

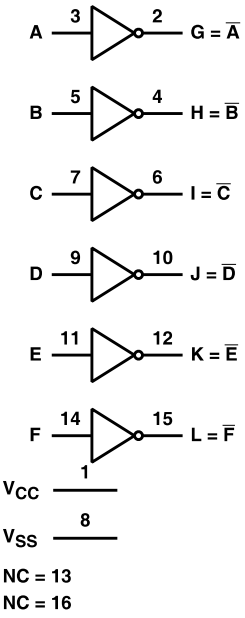
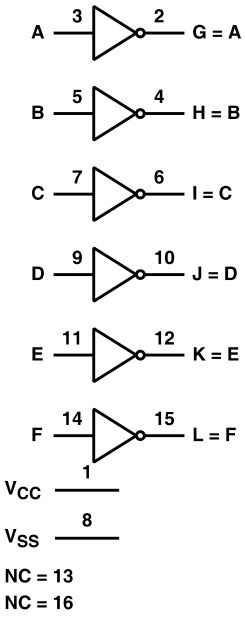
**CD4049UB (TOP VIEW)**




**CD4050B (TOP VIEW)**



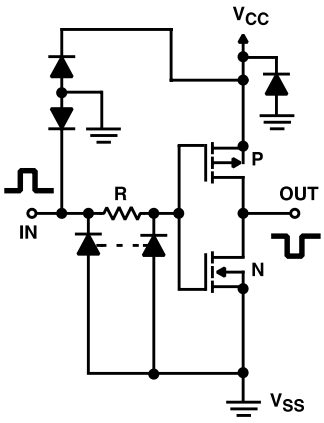
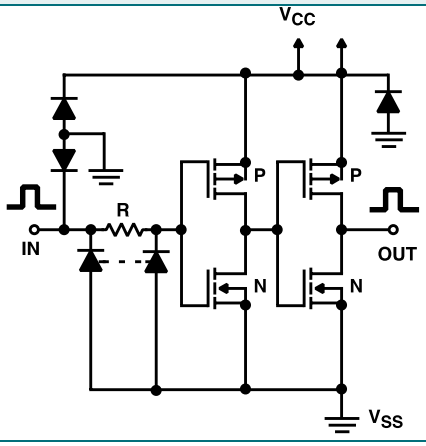
## 6. Functional Block Diagrams

| CD4049UB | CD4050B |
|---|---|
|  |  |





## 7. Schematic Diagrams

| CD4049UB IDENTICAL UNITS | CD4050B IDENTICAL UNITS |
|---|---|
|  |  |





## 8. Absolute Maximum Ratings

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ to $V_{SS}$ | –0.5 | 20 | V |
| DC input current, $I_{IK}$ | Any one input | | ±10 | mA |
| Lead temperature (soldering, 10 s) | SOIC, lead tips only | | 265 | °C |
| Junction temperature, $T_J$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

## 9. Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_A$ | Operating temperature | –55 | 125 | °C |

## 10. DC Electrical Specifications

| PARAMETER | TEST CONDITIONS | | | LIMITS AT INDICATED TEMPERATURE (°C) | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 25 | | | |
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{CC}$ (V) | -55 | -40 | 85 | 125 | MIN | TYP | MAX | |
| Quiescent Device Current $I_{DD}$ (Max) | - | 0,5 | 5 | 1 | 1 | 30 | 30 | - | 0.02 | 1 | mA |
| | - | 0,10 | 10 | 2 | 2 | 60 | 60 | - | 0.02 | 2 | mA |
| | - | 0,15 | 15 | 4 | 4 | 120 | 120 | - | 0.02 | 4 | mA |
| | - | 0,20 | 20 | 20 | 20 | 600 | 600 | - | 0.04 | 20 | mA |
| Output Low (Sink) Current $I_{OL}$ (Min) | 0.4 | 0,5 | 4.5 | 3.3 | 3.1 | 2.1 | 1.8 | 2.6 | 5.2 | - | mA |
| | 0.4 | 0,5 | 5 | 4 | 3.8 | 2.9 | 2.4 | 3.2 | 6.4 | - | mA |
| | 0.5 | 0,10 | 10 | 10 | 9.6 | 6.6 | 5.6 | 8 | 16 | - | mA |
| | 1.5 | 0,15 | 15 | 26 | 25 | 20 | 18 | 24 | 48 | - | mA |
| Output High (Source) Current $I_{OH}$ (Min) | 4.6 | 0,5 | 5 | -0.81 | -0.73 | -0.58 | -0.48 | -0.65 | -1.2 | - | mA |
| | 2.5 | 0,5 | 5 | -2.6 | -2.4 | -1.9 | -1.55 | -2.1 | -3.9 | - | mA |
| | 9.5 | 0,10 | 10 | -2.0 | -1.8 | -1.35 | -1.18 | -1.65 | -3.0 | - | mA |
| | 13.5 | 0,15 | 15 | -5.2 | -4.8 | -3.5 | -3.1 | -4.3 | -8.0 | - | mA |
| Out Voltage Low Level $V_{OL}$ (Max) | - | 0,5 | 5 | 0.05 | 0.05 | 0.05 | 0.05 | - | 0 | 0.05 | V |
| | - | 0,10 | 10 | 0.05 | 0.05 | 0.05 | 0.05 | - | 0 | 0.05 | V |
| | - | 0,15 | 5 | 0.05 | 0.05 | 0.05 | 0.05 | - | 0 | 0.05 | V |
| Output Voltage High Level $V_{OH}$ (Min) | - | 0,5 | 5 | 4.95 | 4.95 | 4.95 | 4.95 | 4.95 | 5 | - | V |
| | - | 0,10 | 10 | 9.95 | 9.95 | 9.95 | 9.95 | 9.95 | 10 | - | V |
| | - | 0,15 | 15 | 14.95 | 14.95 | 14.95 | 14.95 | 14.95 | 15 | - | V |
| Input Low Voltage $V_{IL}$ (Max) CD4049UB | 4.5 | - | 5 | 1 | 1 | 1 | 1 | - | - | 1 | V |
| | 9 | - | 10 | 2 | 2 | 2 | 2 | - | - | 2 | V |
| | 13.5 | - | 15 | 2.5 | 2.5 | 2.5 | 2.5 | - | - | 2.5 | V |
| Input Low Voltage $V_{IL}$ (Max) CD4050B | 0.5 | - | 5 | 1.5 | 1.5 | 1.5 | 1.5 | - | - | 1.5 | V |
| | 1 | - | 10 | 3 | 3 | 3 | 3 | - | - | 3 | V |
| | 1.5 | - | 15 | 4 | 4 | 4 | 4 | - | - | 4 | V |
| Input High Voltage $V_{IH}$ Min CD4049UB | 0.5 | - | 5 | 4 | 4 | 4 | 4 | 4 | - | - | V |
| | 1 | - | 10 | 8 | 8 | 8 | 8 | 8 | - | - | V |
| | 1.5 | - | 15 | 12.5 | 12.5 | 12.5 | 12.5 | 12.5 | - | - | V |
| Input High Voltage $V_{IH}$ Min CD4050B | 4.5 | - | 5 | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 | - | - | V |
| | 9 | - | 10 | 7 | 7 | 7 | 7 | 7 | - | - | V |
| | 13.5 | - | 15 | 11 | 11 | 11 | 11 | 11 | - | - | V |
| Input Current $I_{IN}$ Max | - | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | - | $\pm10^{-5}$ | ±0.1 | mA |

## 11. AC Electrical Specifications

| PARAMETER | TEST CONDITIONS | | LIMITS (ALL PACKAGES) | | UNITS |
|---|---|---|---|---|---|
| | $V_{IN}$ | $V_{CC}$ | TYP | MAX | |
| Propagation Delay Time Low to High, $t_{PLH}$ CD4049UB | 5 | 5 | 60 | 120 | ns |
| | 10 | 10 | 32 | 65 | ns |
| | 10 | 5 | 45 | 90 | ns |
| | 15 | 15 | 25 | 50 | ns |
| | 15 | 5 | 45 | 90 | ns |
| Propagation Delay Time Low to High, $t_{PLH}$ CD4050B | 5 | 5 | 70 | 140 | ns |
| | 10 | 10 | 40 | 80 | ns |
| | 10 | 5 | 45 | 90 | ns |
| | 15 | 15 | 30 | 60 | ns |
| | 15 | 5 | 40 | 80 | ns |
| Propagation Delay Time High to Low, $t_{PHL}$ CD4049UB | 5 | 5 | 32 | 65 | ns |
| | 10 | 10 | 20 | 40 | ns |
| | 10 | 5 | 15 | 30 | ns |
| | 15 | 15 | 15 | 30 | ns |
| | 15 | 5 | 10 | 20 | ns |
| Propagation Delay Time High to Low, $t_{PHL}$ CD4050B | 5 | 5 | 55 | 110 | ns |
| | 10 | 10 | 22 | 55 | ns |
| | 10 | 5 | 50 | 100 | ns |
| | 15 | 15 | 15 | 30 | ns |
| | 15 | 5 | 50 | 100 | ns |
| Transition Time, Low to High, $t_{TLH}$ | 5 | 5 | 80 | 160 | ns |
| | 10 | 10 | 40 | 80 | ns |
| | 15 | 15 | 30 | 60 | ns |
| Transition Time, High to Low, $t_{THL}$ | 5 | 5 | 30 | 60 | ns |
| | 10 | 10 | 20 | 40 | ns |
| | 15 | 15 | 15 | 30 | ns |
| Input Capacitance, $C_{IN}$ CD4049UB | - | - | 15 | 22.5 | pF |
| Input Capacitance, $C_{IN}$ CD4050B | - | - | 5 | 7.5 | pF |

## 12. Typical Performance Curves

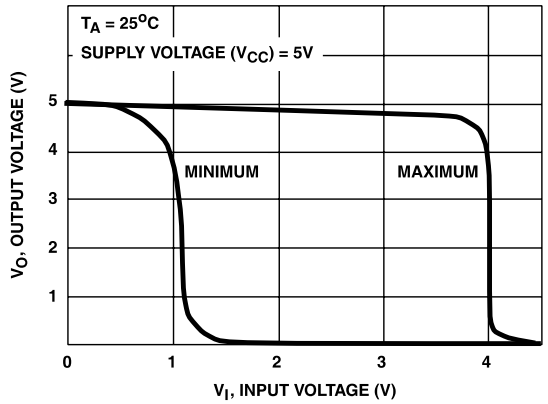



FIGURE 2. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS FOR CD4049UB

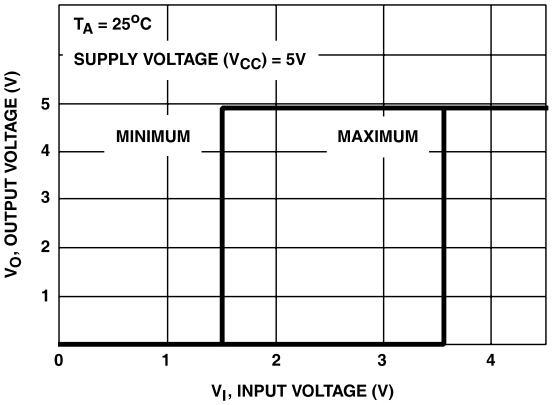



FIGURE 3. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS FOR CD4050B

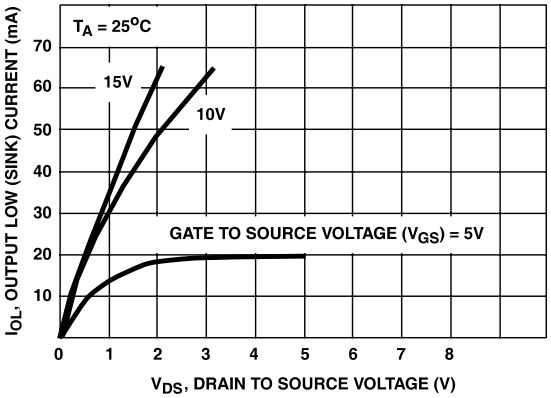



FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

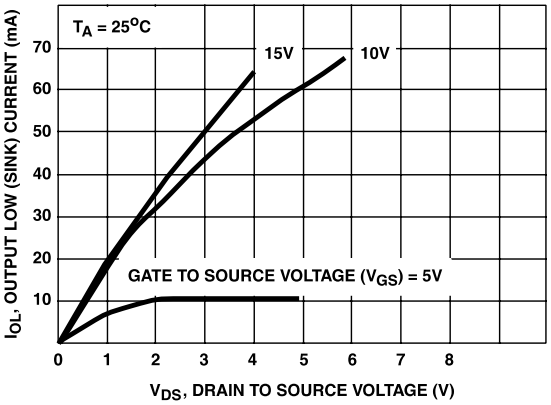



FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT DRAIN CHARACTERISTICS

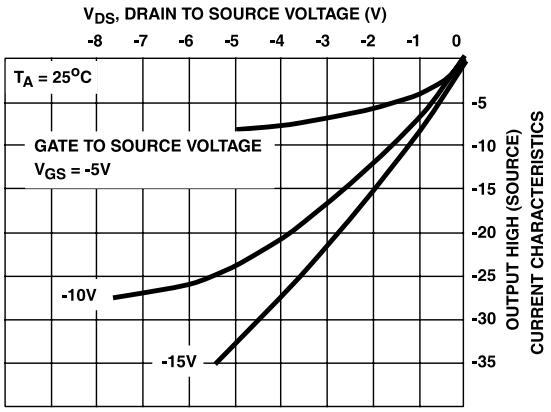



FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

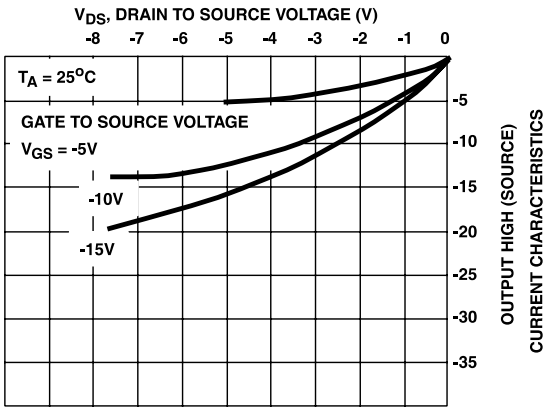



FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

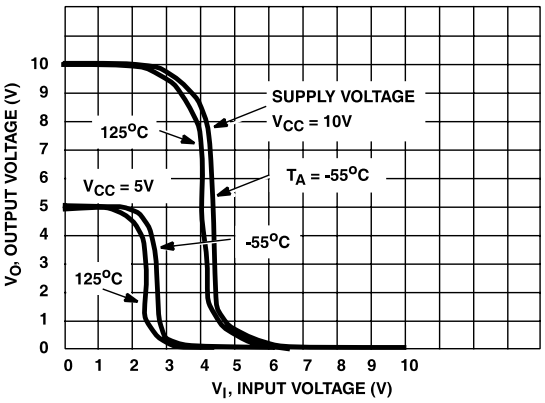



FIGURE 8. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR CD4049UB

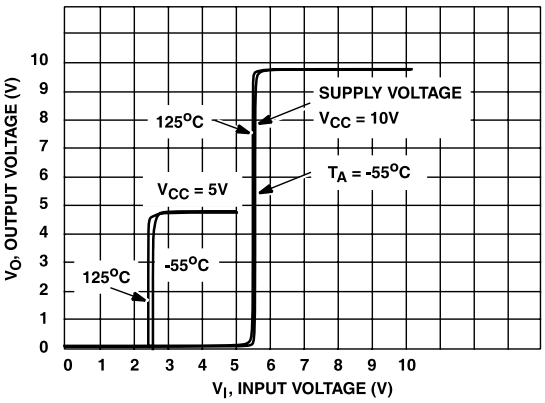



FIGURE 9. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR CD4050B

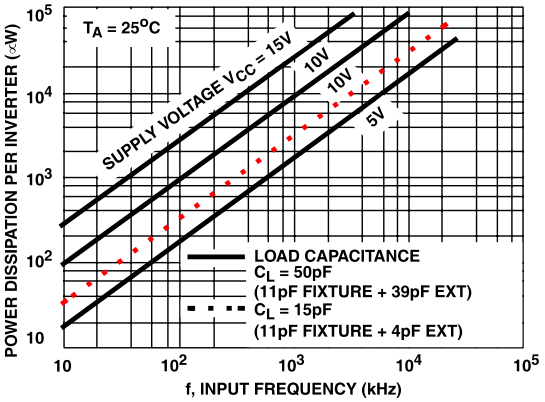



FIGURE 10. TYPICAL POWER DISSIPATION vs FREQUENCY CHARACTERISTICS

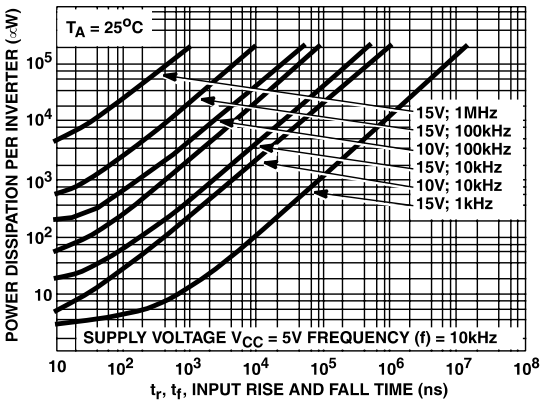



FIGURE 11. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER FOR CD4049UB

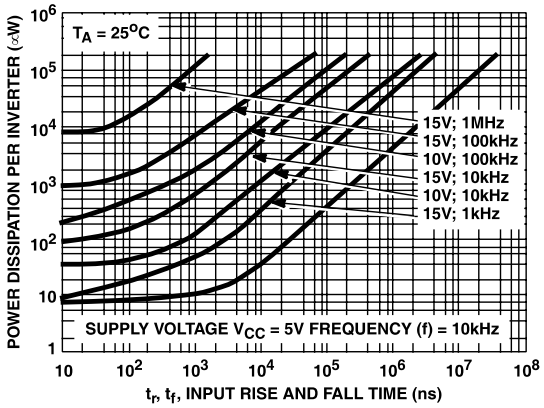



FIGURE 12. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTERFOR CD4050B

## 13. Test Circuts

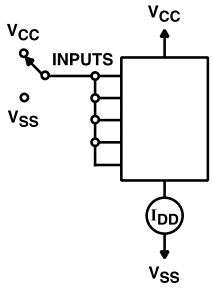
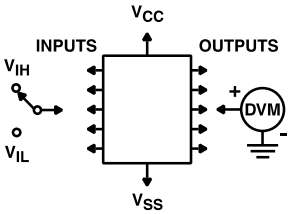
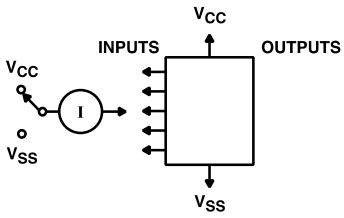



FIGURE 13. QUIESCENT DEVICE CURRENT TEST CIRCUIT



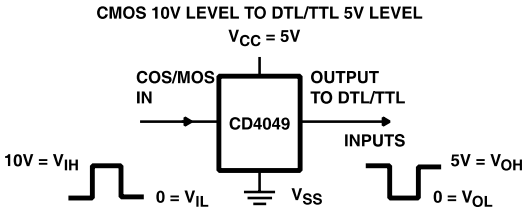

NOTE: Test any one input with other inputs at $V_{CC}$ or $V_{SS}$.

FIGURE 14. INPUT VOLTAGE TEST CIRCUIT



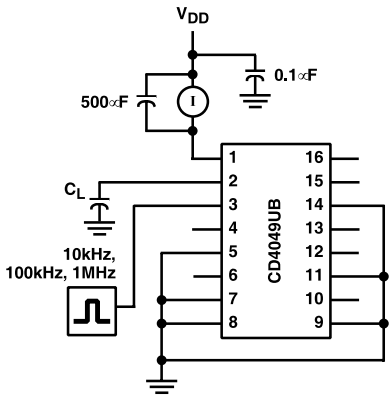

NOTE: Measure inputs sequentially, to both $V_{CC}$ and $V_{SS}$ connect all unused inputs to either $V_{CC}$ or $V_{SS}$.

FIGURE 15. INPUT CURRENT TEST CIRCUIT




In Terminal - 3, 5, 7, 9, 11, or 14
Out Terminal - 2, 4, 6, 10, 12 or 15
$V_{CC}$ Terminal - 1
$V_{SS}$ Terminal - 8

FIGURE 16. LOGIC LEVEL CONVERSION APPLICATION

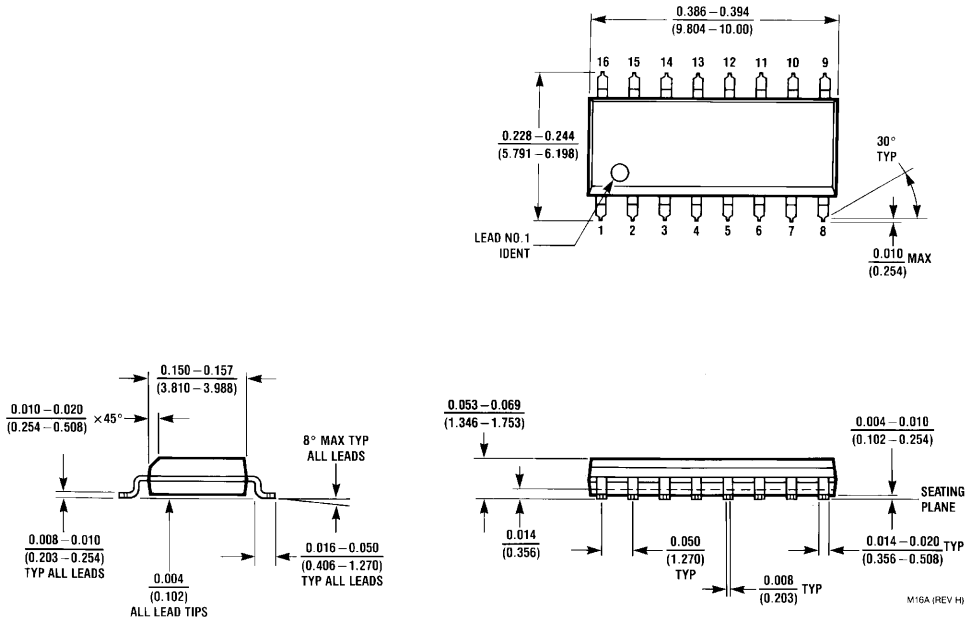



$C_L$ INCLUDES FIXTURE CAPACITANCE

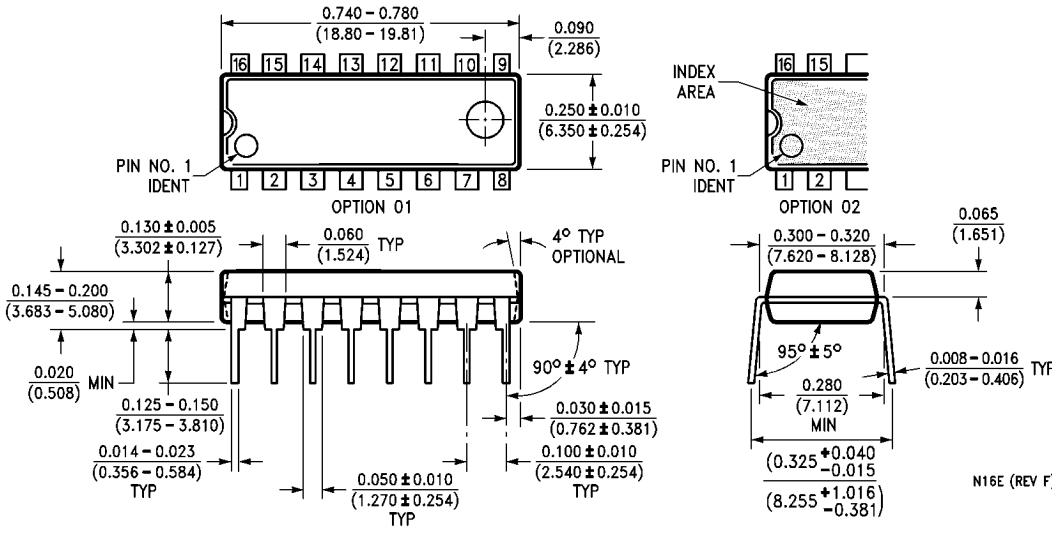
FIGURE 17. DYNAMIC POWER DISSIPATION TEST CIRCUITS

# 14. Package outlines

**SOIC-16**




**DIP-16**



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