

CD4069UB CMOS hex inverter

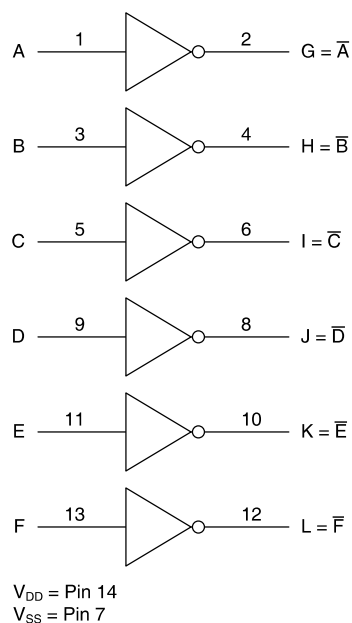
1. Description

The CD4069UB types consist of six inverter circuits. These devices are intended for all general-purpose inverter applications where the medium-power TTL drive and logic-level-conversion capabilities of circuits are not required. Each of the six inverters is a single stage.

2. Features

- Wide supply voltage range: 3.0V ~ 15V.
- High noise immunity: 0.45 V_{DD} typ.
- Low Power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS.

5. Functional Block Diagram



3. Applications

- Logic inversion
- Pulse shaping
- Oscillators
- High-input-impedance amplifiers

4. Ordering Information

P/N	Package	Marking	Packing
CD4069UBN	DIP-14	CD4069UB	Tube
CD4069UBM	SOIC-14	CD4069UB	Reel

6. Pin Configuration

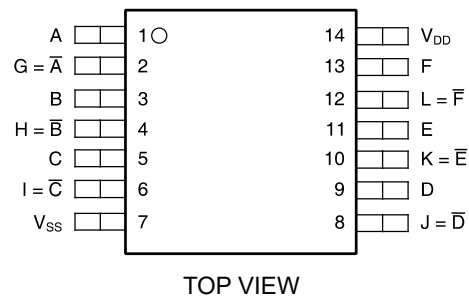


Table 1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	1	I	A input
B	3	I	B input
C	5	I	C input
D	9	I	D input
E	11	I	E input
F	13	I	F input
G = A	2	O	G output
H = B	4	O	H output
I = C	6	O	I output
J = D	8	O	J output
K = E	10	O	K output
L = F	12	O	L output
V _{DD}	14	—	Positive supply
V _{SS}	7	—	Negative supply

7. Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
V _{DD}	DC Supply Voltage	-0.5	18	V
V _{IN}	Input Voltage	-0.5	V _{DD} + 0.5	V
T _S	Storage Temperature Range	-65 ~ +150	+150	°C
P _D	Power Dissipation	DIP-14	700	mW
		SOP-14	500	
T _J	Junction Temperature		125	°C
T _{OPR}	Operating Temperature	-20	+85	°C
T _{STG}	Storage Temperature	-40	+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

8. Recommended Operating Conditions

(V_{SS}=0V)

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage	V _{DD}	3 ~ 15	V
Input Voltage	V _{IN}	0 ~ V _{DD}	V
Operating Temperature	T _A	-40 ~ 85	°C

9. Dc Electrical Characteristics

($V_{SS}=0V$, $T_A=25^{\circ}C$, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Device Current	I_{DD}	$V_{DD}=5V$, $V_{IN}=V_{DD}$ or V_{SS}			1.0	μA
		$V_{DD}=10V$, $V_{IN}=V_{DD}$ or V_{SS}			2.0	μA
		$V_{DD}=15V$, $V_{IN}=V_{DD}$ or V_{SS}			4.0	μA
Low Level Output Voltage	V_{OL}	$ I_O < 1\mu A$	$V_{DD}=5V$	0	0.05	V
			$V_{DD}=10V$	0	0.05	V
			$V_{DD}=15V$	0	0.05	V
High Level Output Voltage	V_{OH}	$ I_O < 1\mu A$	$V_{DD}=5V$	4.95		V
			$V_{DD}=10V$	9.95		V
			$V_{DD}=15V$	14.95		V
Low Level Input Voltage	V_{IL}	$ I_O < 1\mu A$	$V_{DD}=5V$, $V_O=4.5V$		1.0	V
			$V_{DD}=10V$, $V_O=9V$		2.0	V
			$V_{DD}=15V$, $V_O=13.5V$		3.0	V
High Level Input Voltage	V_{IH}	$ I_O < 1\mu A$	$V_{DD}=5V$, $V_O=0.5V$	4.0		V
			$V_{DD}=10V$, $V_O=1V$	8.0		V
			$V_{DD}=15V$, $V_O=1.5V$	12.0		V
Low Level Output Current	I_{OL}	$V_{DD}=5V$, $V_O=0.4V$	0.44	0.88		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.1	2.25		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.0	8.8		mA
High Level Output Current	I_{OH}	$V_{DD}=5V$, $V_O=4.6V$	-0.44	-0.88		mA
		$V_{DD}=10V$, $V_O=9.5V$	-1.1	-2.25		mA
		$V_{DD}=15V$, $V_O=13.5V$	-3.0	-8.8		mA
Input Current	I_{IN}	$V_{DD}=15V$, $V_{IN}=0V$		-10^{-5}	-0.30	μA
		$V_{DD}=15V$, $V_{IN}=15V$		10^{-5}	0.30	μA

10. Ac Electrical Characteristics

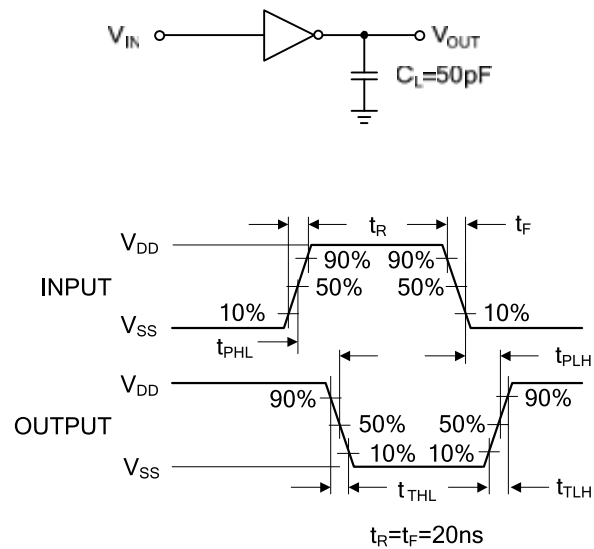
($T_A=25^{\circ}\text{C}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$, t_R and $t_F \leq 20\text{ ns}$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time from Input to Output	t_{PHL} or t_{PLH}	$V_{DD}=5\text{V}$		50	90	ns
		$V_{DD}=10\text{V}$		30	60	ns
		$V_{DD}=15\text{V}$		25	50	ns
Transition Time	t_{THL} or t_{TLH}	$V_{DD}=5\text{V}$		80	150	ns
		$V_{DD}=10\text{V}$		50	100	ns
		$V_{DD}=15\text{V}$		40	80	ns
Average Input Capacitance	C_{IN}	Any Gate		6	15	pF
Power Dissipation Capacitance	C_{PD}	Any Gate		12		pF

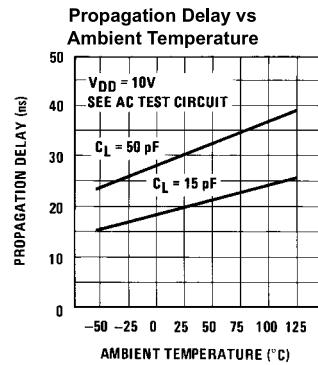
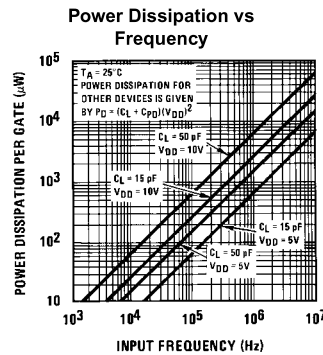
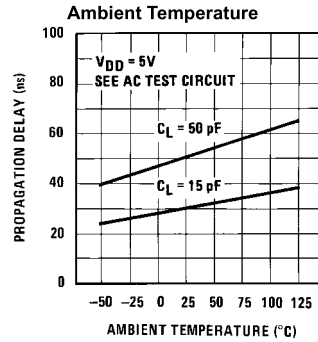
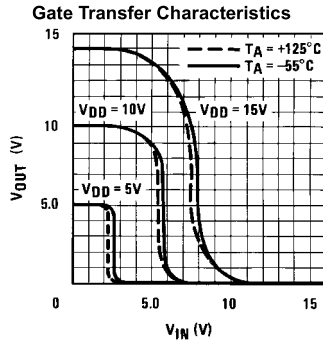
Notes:

- AC Parameters are guaranteed by DC correlated testing.
- I_{OH} and I_{OL} are tested one output at a time.
- C_{PD} determines the no load AC power consumption of any CMOS device.

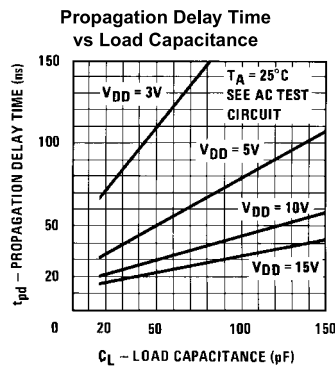
11. Ac Test Circuits and Switching Time Waveforms



12. Typical Performance Characteristics

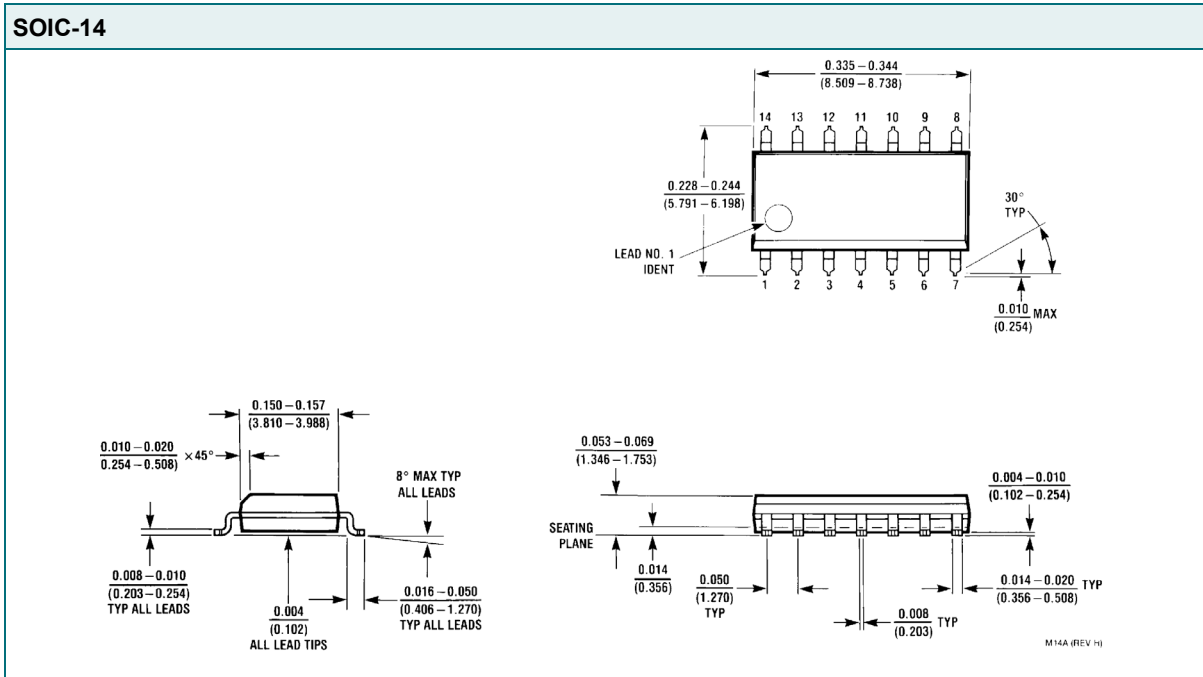


Propagation Delay vs

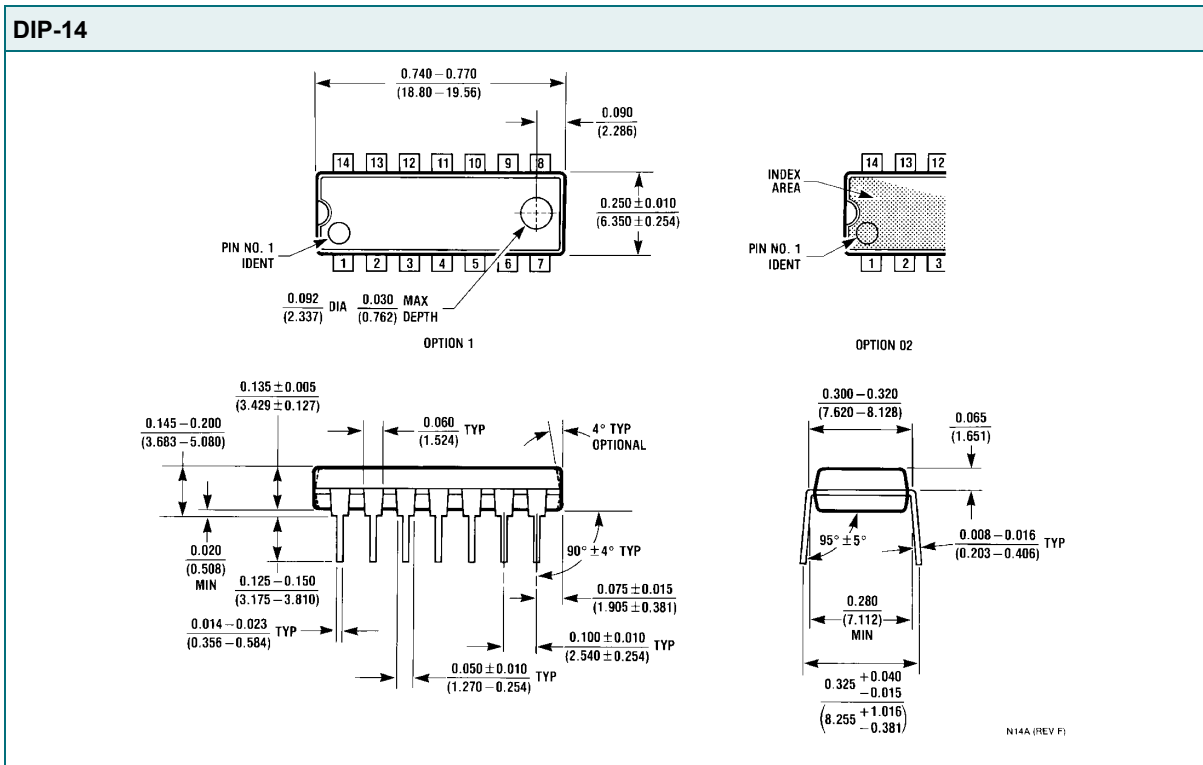


13. Package outlines

SOIC-14



DIP-14



14. Disclaimers

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